



PTO/SB/08A (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/618,462
Filing Date	07/11/2003
First Named Inventor	Guangming Yin
Art Unit	2817
Examiner Name	Nguyen, Patricia T.
Attorney Docket Number	BP1817CON1

Sheet 1 of 4

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
PN		US- 5,345,449	09-06-1994	Inmos Limited	
PN		US- 5,420,529	05-30-1995	Northern Telecom Limited	
PN		US- 5,675,584	10-07-1997	Sun Microsystems, Inc.	
PN		US- 5,724,361	03-03-1998	LSI Logic Corporation	
PN		US- 5,767,699	06-16-1998	Sun Microsystems, Inc.	
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PN		US- 6,038,254	03-14-2000		
PN		US- 6,061,747	05-09-2000	LSI Logic Corporation	
PN		US- 6,094,074	07-25-2000	Seiko Epson Corporation	
PN		US- 6,188,339 B1	02-13-2001	Fuji Photo Film Co., Ltd.	
PN		US- 6,194,950 B1	02-27-2001	Lucent Technologies Inc.	
PN		US- 6,222,380 B1	04-24-2001		
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PN		US- 6,463,092 B1	10-08-2002	Silicon Image, Inc.	
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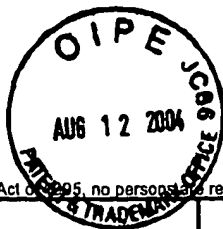
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

Examiner Signature	Patricia Nguyen	Date Considered	10/25/2004
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of

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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PN		MIZUNO, A GHz MOS Adaptive Pipeline Technique Using MOS Current-Mode Logic, IEEE Journal of Solid-State Circuits, vol. 31, No. 6, pp 784-791 (June 1996)	
PN		KLOSE, Process-Optimization for Sub-30ps BiCMOS Technologies for Mixed ECL/CMOS Applications, IEEE 1991	
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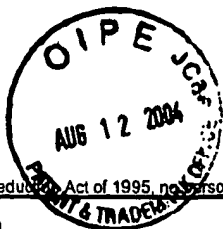
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Nguyen, Patricia T.

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PN		LEE et al., A CMOS Serial Link for 1 Gbaud Fully Duplexed Data Communication, 1994 Symposium on VLSI Circuits Digest of Technical Papers, pp.125-26	
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PN		DJAHANSHAH et al., High-speed ECL-Compatible Serial I/O in 0.35µm CMOS, IEEE 1998	
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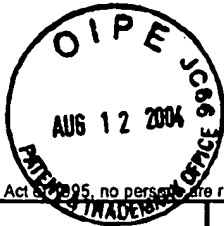
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PN		BAUMERT et al., A Monolithic 50-200 MHz CMOS Clock Recovery and Retiming Circuit, IEEE 1989 Custom Integrated Circuits Conference pp.14.5.1-14.5.4. (May 1989)	

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